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Analog/Digital Converters

Introduction

Robotics is at the frontier of technology today and there is a lot of investment made in robotic research because of the potential for robots to do tasks faster and cheaper than humans. However, in order for a robot to interact with the world around it, the robot requires sensors which often output analog signals. Analog/Digital Converters, also known as ADCs, allow robots to read and process these sensor analog signals. This technical review briefly summarizes some commercial applications and products of ADCs, the technology underlying ADCs, as well as how ADCs are implemented through hardware.

Commercial Applications and Products of ADCs

ADCs are used in any application that requires analog sensor values to be converted into digital values for digital processing. For example, digital cameras use image sensors to convert the light intensity measured in a picture taken to an analog voltage, and thus an ADC is used to convert the analog voltage into a digital signals. Once in digital form, the pictures can be stored digitally and digital modifications such as color filters can be made. Another example of ADC application is that music is often wanted in digital form so that it can edited and can also be cheaply distributed through the internet. However, music recording is often done through microphones that detect sound through mechanical vibrations and then convert the sound to an analog current, which in-turn can be converted into a voltage. Thus, an ADC is used to convert the analog voltage into a digital signal.

The LTC2378-20 is a low-priced 1 channel SAR architecture ADC made by Linear Technology [1] that costs $29.50 [2]. It has a resolution of 20 bits, an input voltage range of 0.5-4.5V, a throughput of 1Msps (Mega samples per second), a max INL (Integral Non-Linearity) of 0.5, an SNR of 104 dB typical at 2kHz, and a power consumption of 21mW typical [1].

The AD1555 in comparison is a mid-priced 2 channel Delta-Sigma architecture ADC made by Analog Devices [3] that costs $74.61 [4]. While its input range is the same as the LTC2378-20, the whole range is shifted to +-2.25V, so it allows for negative ADC input. While its resolution of 24 bits is higher than that of the LTC2378-20, it has a lower throughput of 256 kSPS. Its SNR is 116.7 dB and its typical power consumption is 96mW typical [4].

The ADS5400 is the most expensive ADC out of the three ADCs mentioned. It is a 1 channel Pipeline architecture ADC made by Texas Instruments that costs $1079.82 [5]. Its input voltage range of 1.75-3.75V for DC signals and 1.25-3.75 for AC signals is smaller than that of the previously mentioned ADCs, and so is its resolution of 12 bits [5]. However, its throughput of 1 Gsps is much faster [5]. It has a high max INL of 4 but has a low SNR of 59.1 dB. For its high throughput, it appropriately has the highest power consumption, 2200mW, of the three ADCs mentioned [5].

Underlying Technology

ADCs convert continuous time and amplitude signals to discrete time and amplitude signals, by sampling the analog values periodically [6]. If an ADC samples at a rate greater than twice the bandwidth of the input analog signal (referred to as the Nyquist frequency), then perfect reconstruction the signal is possible assuming an ideal ADC and neglecting quantization error [7]. There are several algorithms/architectures that can be implemented for ADCs, but this paper will go over only two common algorithms.

The Successive Approximation algorithm (SAR) works by narrowing down the range that the input analog signal can be in through comparing the analog input to the midpoint of the possible input range, shortening the possible input range of values to which ever half of the range that the analog input is on, and then repeating the process [8]. SAR ADCs usually have less than 4 Msps throughput, have less than 18 bits resolution, and have low cost and low power that scales with sample rate [9].

In the Delta-Sigma algorithm, a modulator samples an input analog signal into a 1-bit stream at a rate much higher than the Nyquist frequency, and then uses a digital/decimation filter to produce a slower, but high-resolution digital output [10]. Delta-Sigma ADC's usually have less than 10 Msps throughput, have less than 31 bits resolution, have moderate cost, as well as a constant power consumption [9].

Some relevant measures of performance include resolution (in bits) which dictate the # of binary bits that can quantize an analog signal [11] and thus the precision of the ADC measurements, throughput rate (in SPS or samples per second) which dictates how fast an ADC can sample and process an input analog signal [11], INL (Integral Nonlinearity) which is the maximum deviation between the ideal transition points and the actual transitions points of the digital output codes of the ADC, SNR (Signal Noise ratio) which is the ratio of ac signal power to noise power below ½ of the sampling frequency of the ADC[11], and power consumption.

Implementation of technology

There are several hardware components used to implement ADCs. Comparators are used in most, if not all, of the ADC architectures to narrow down what binary code an input analog value is closest to. DACs work in conjunction with comparators by converting binary codes to analog voltages to use as the reference voltage of the comparator. Registers are used to store the binary mapping of input analog signals and an integrator is used as part of some algorithms. Some parameters to consider when looking to practically implement an ADC in a design include # of channels and output communication protocol [6].

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